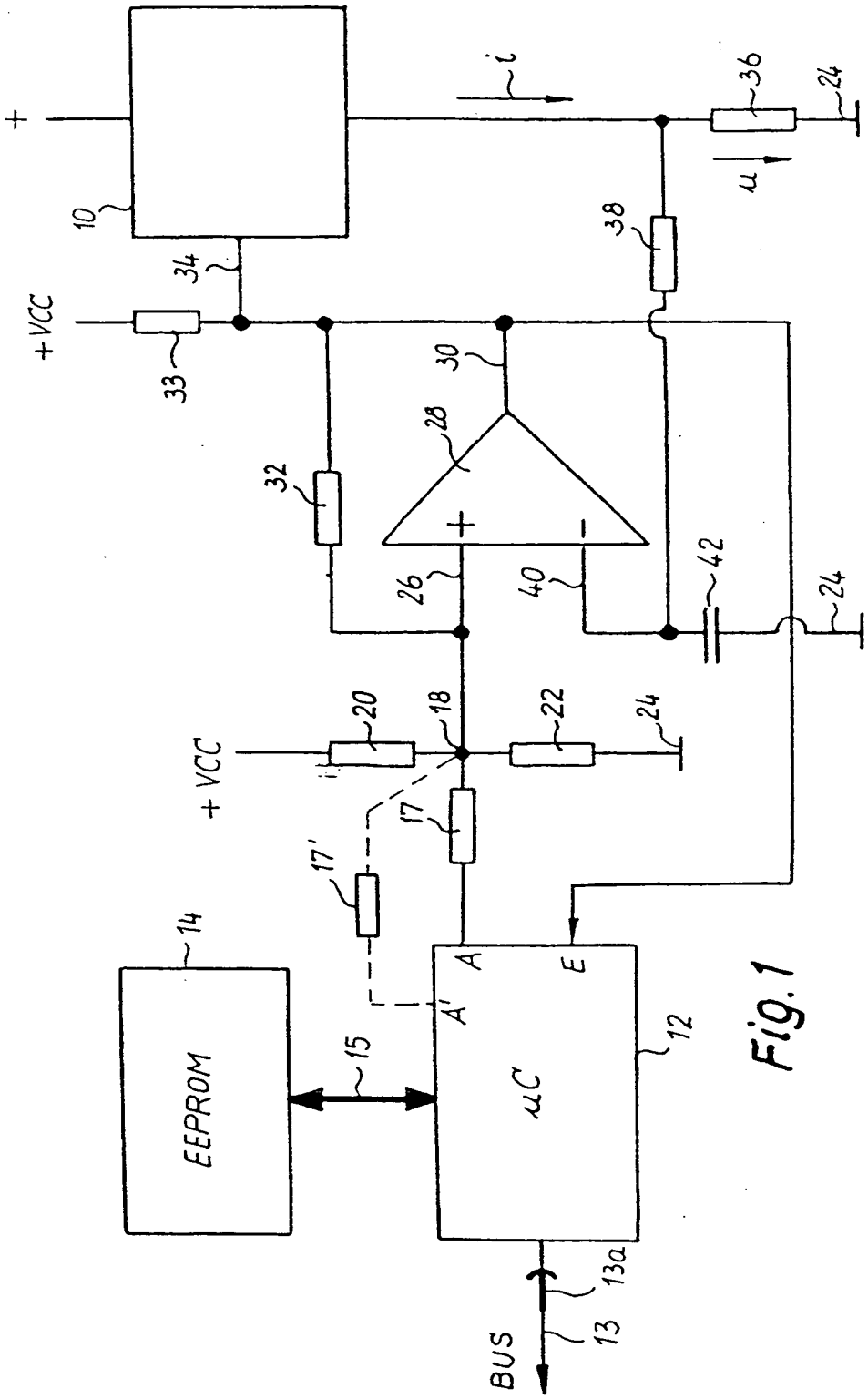

+
10
i
36
24
u
38
34
+VCC
33
30
28
32
26
40
42
24
20
18
22
24
+VCC
17
17'
14
A
A'
E
15
EEPROM
µC
12
BUS
13a
13

Fig. 1

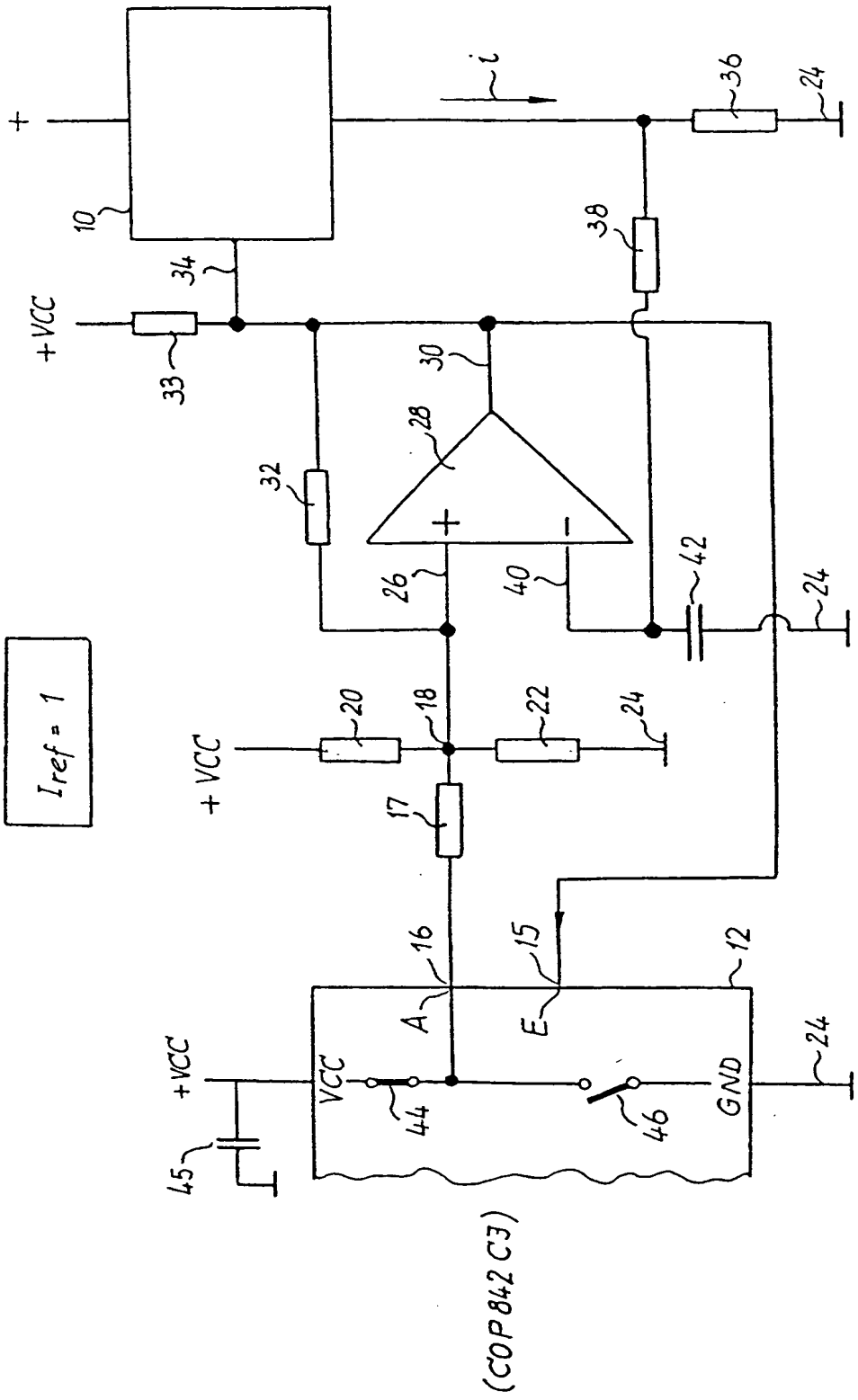


Fig. 2

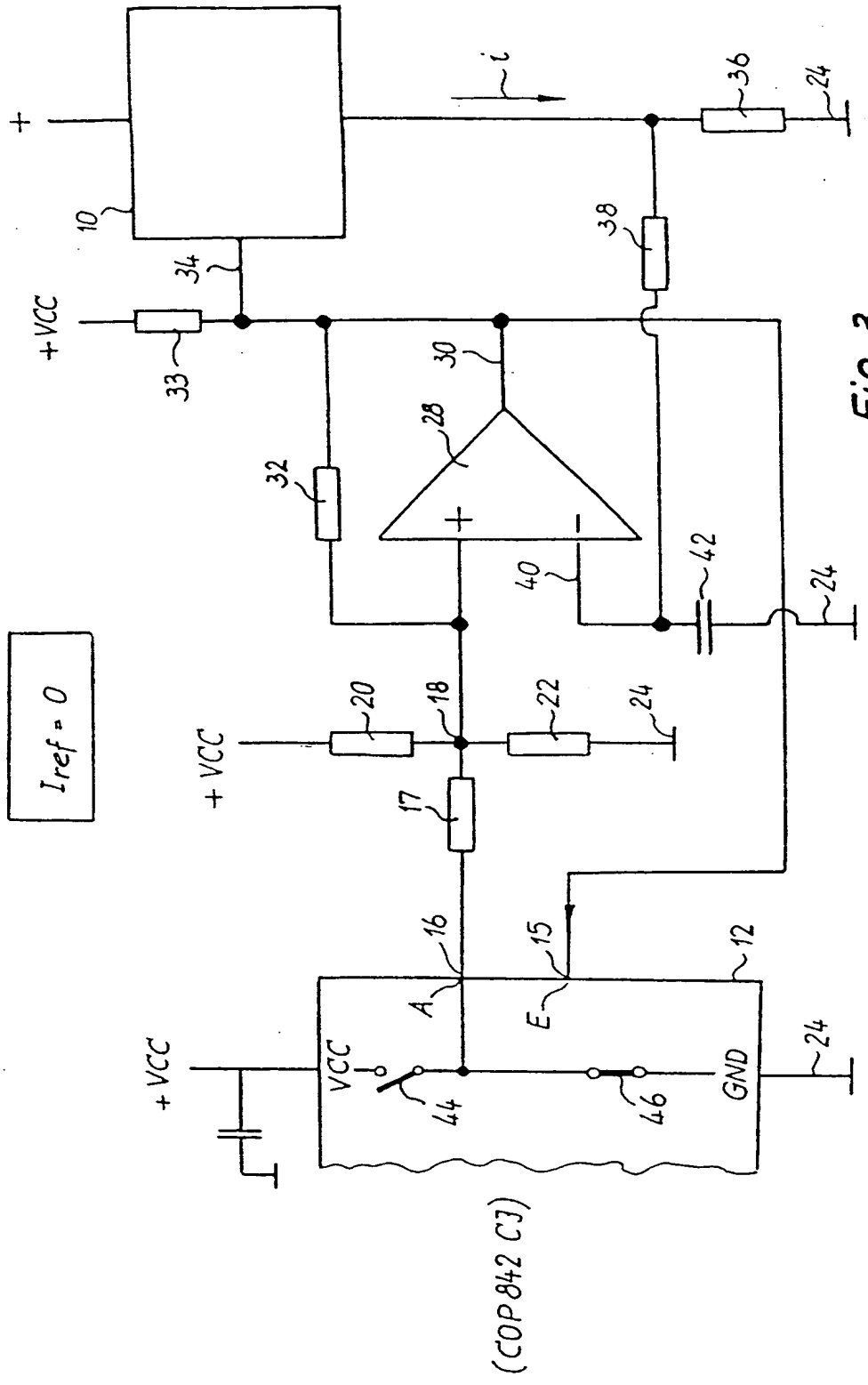

+
10
i
36
24
38
34
+VCC
33
30
28
32
+
-
42
40
24
Iref = 0
+VCC
20
18
22
24
17
16
15
12
A
E
+VCC
VCC
GND
24
44
46
(COP842 C3)

Fig.3

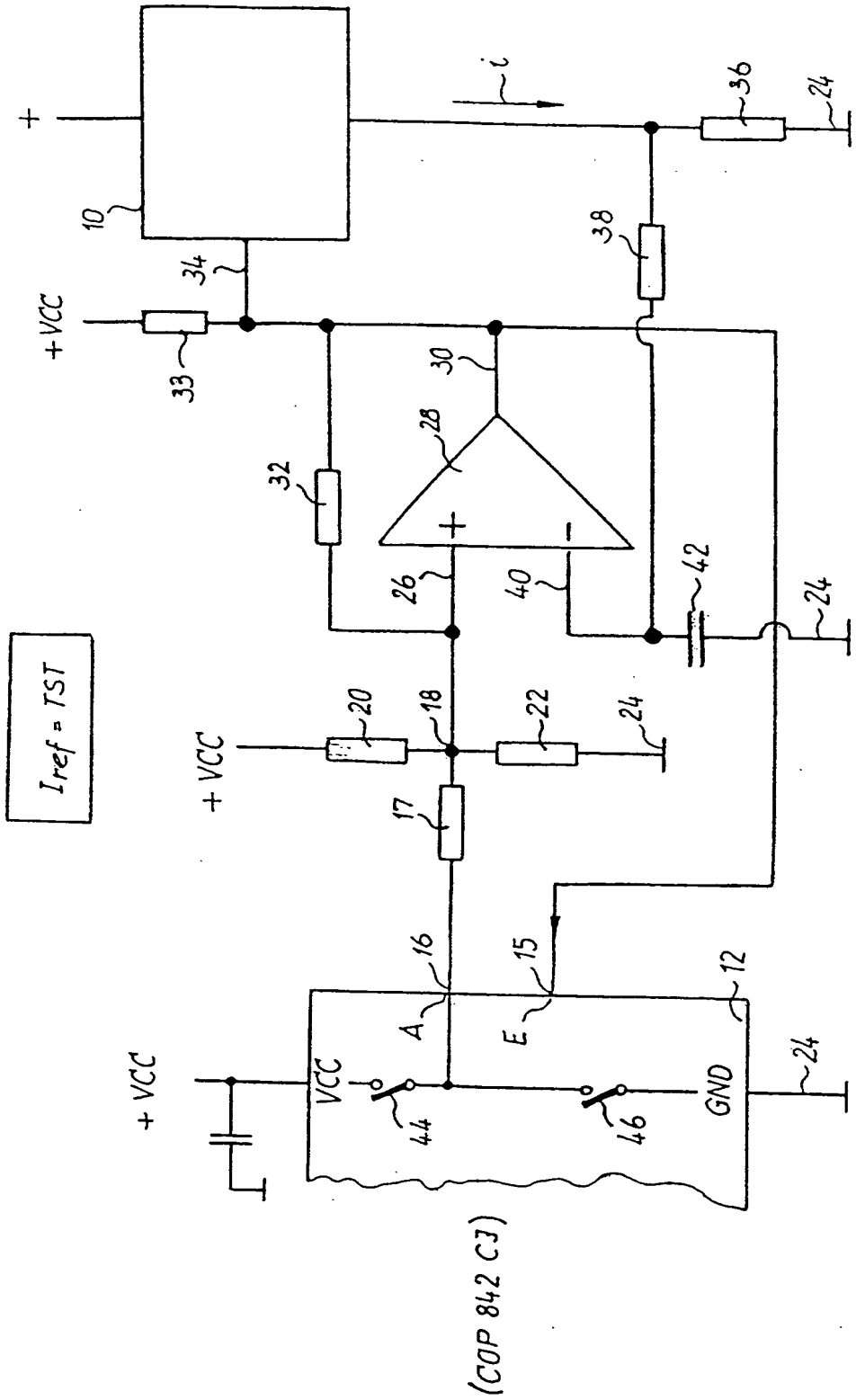

+
10
i
36
24
38
34
+VCC
33
30
28
32
26
40
42
24
Iref = TST
+VCC
20
18
22
24
17
16
15
12
A
E
+VCC
VCC
44
46
GND
24
(COP 842 CJ)

Fig. 4

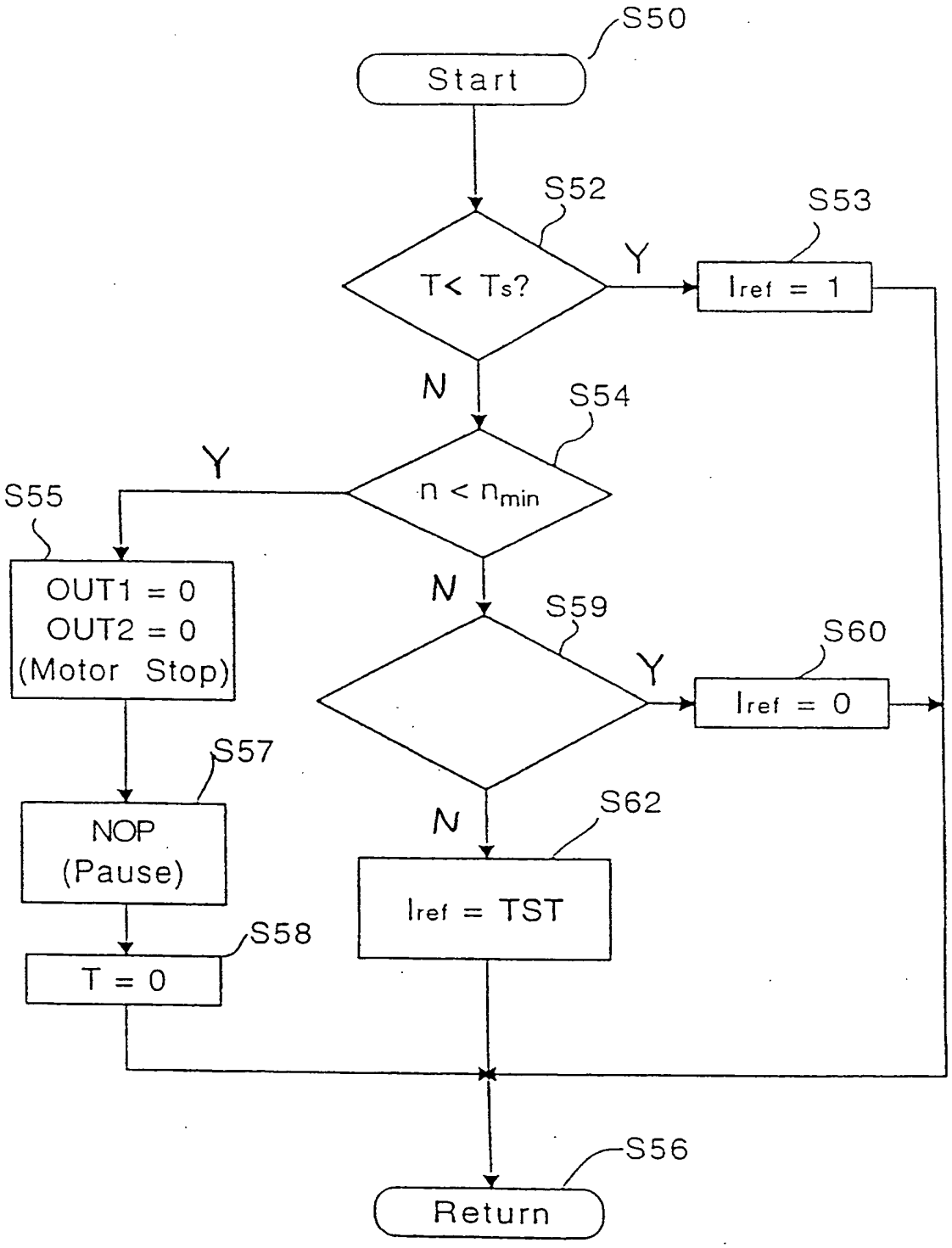

S50
Start
S52
T< Ts?
Y
S53
Iref = 1
N
S54
n < nmin
Y
S55
OUT1 = 0
OUT2 = 0
(Motor Stop)
N
S59
Y
S60
Iref = 0
S57
NOP
(Pause)
N
S62
Iref = TST
S58
T = 0
S56
Return

Fig. 5

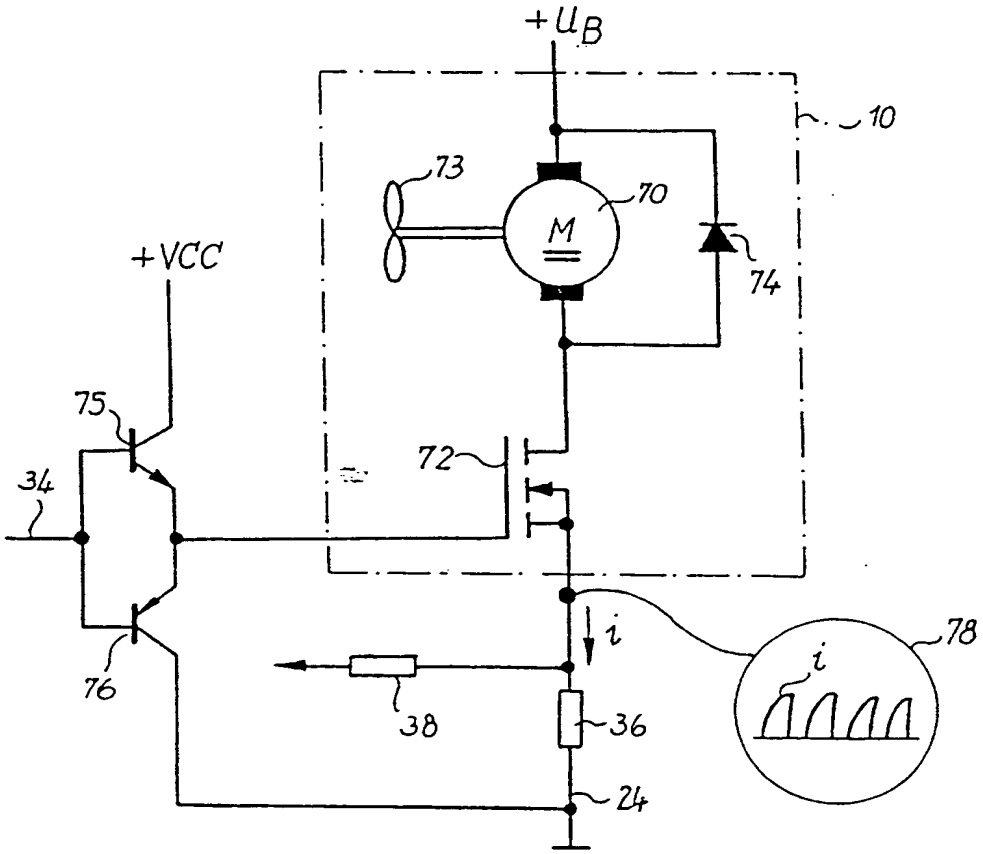


Fig. 6

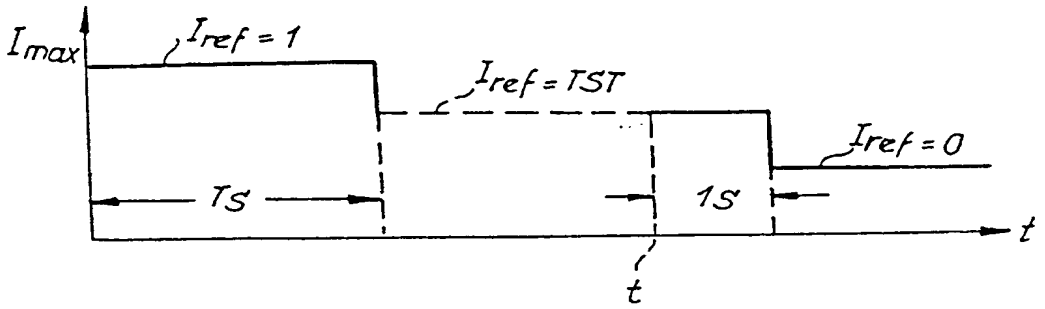

Imax
Iref = 1
Iref = TST
Iref = 0
TS
1S
t
t

Fig. 7

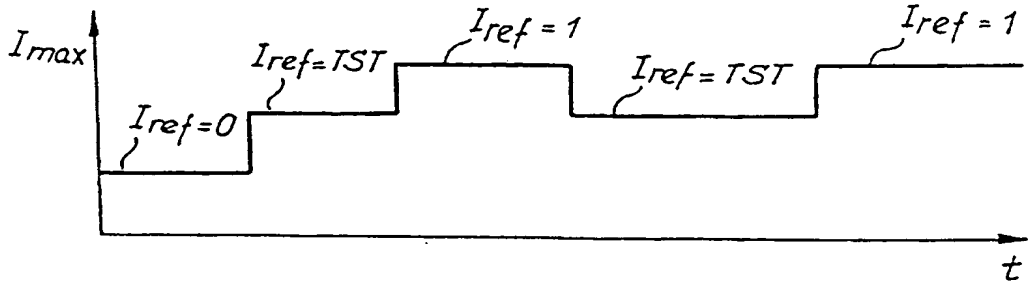

Imax
Iref = 1
Iref = 1
Iref = TST
Iref = TST
Iref = 0
t

Fig. 8

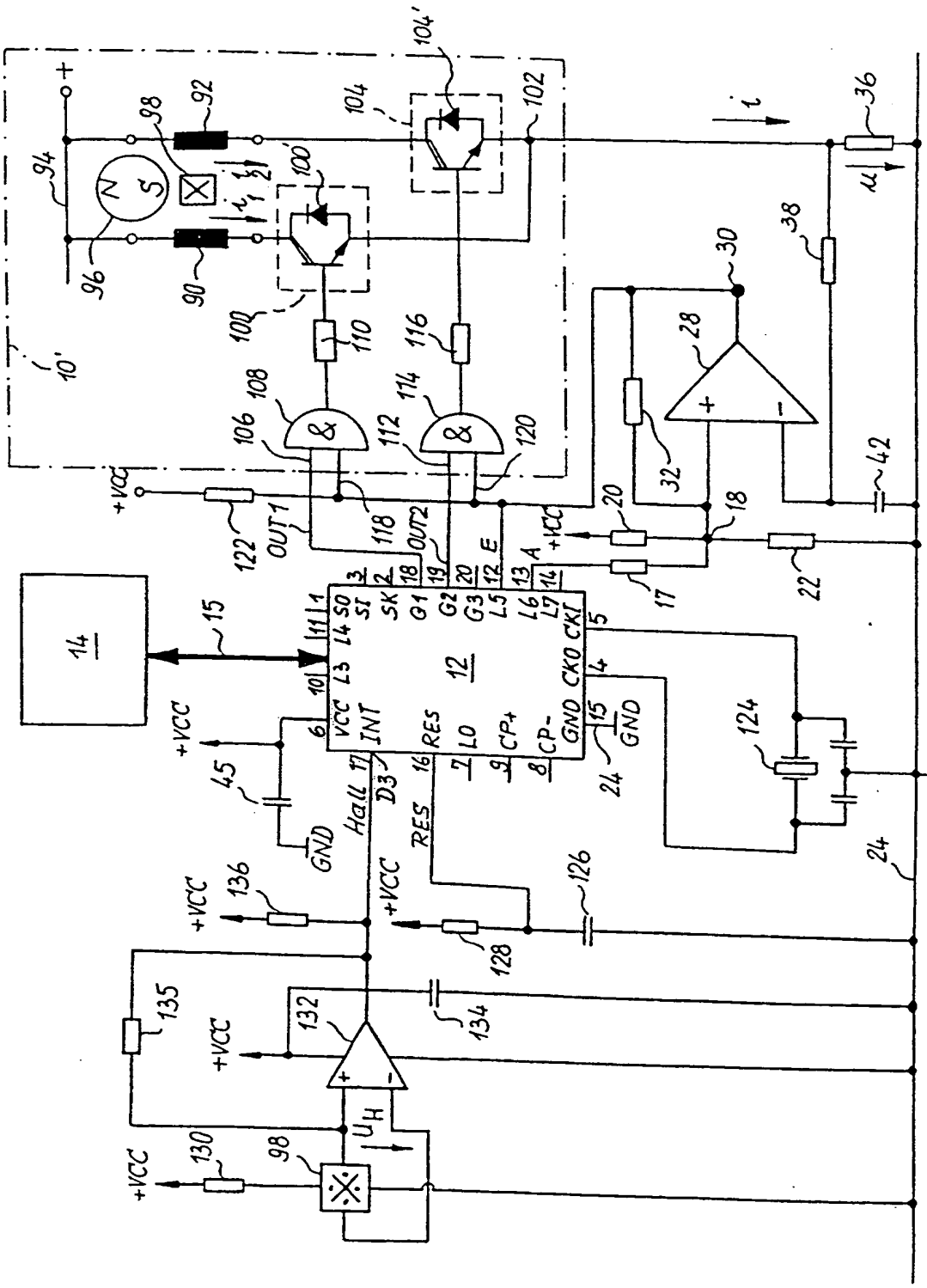

10'
14
15
12
+VCC
GND
OUT1
OUT2
Hall
RES
D3
INT
VCC
GND
SI
SO
SK
CKI
CKO
G1
G2
G3
L3
L4
L5
L6
L7
E
A
CP+
CP-
LO
U_H
i

Fig. 9

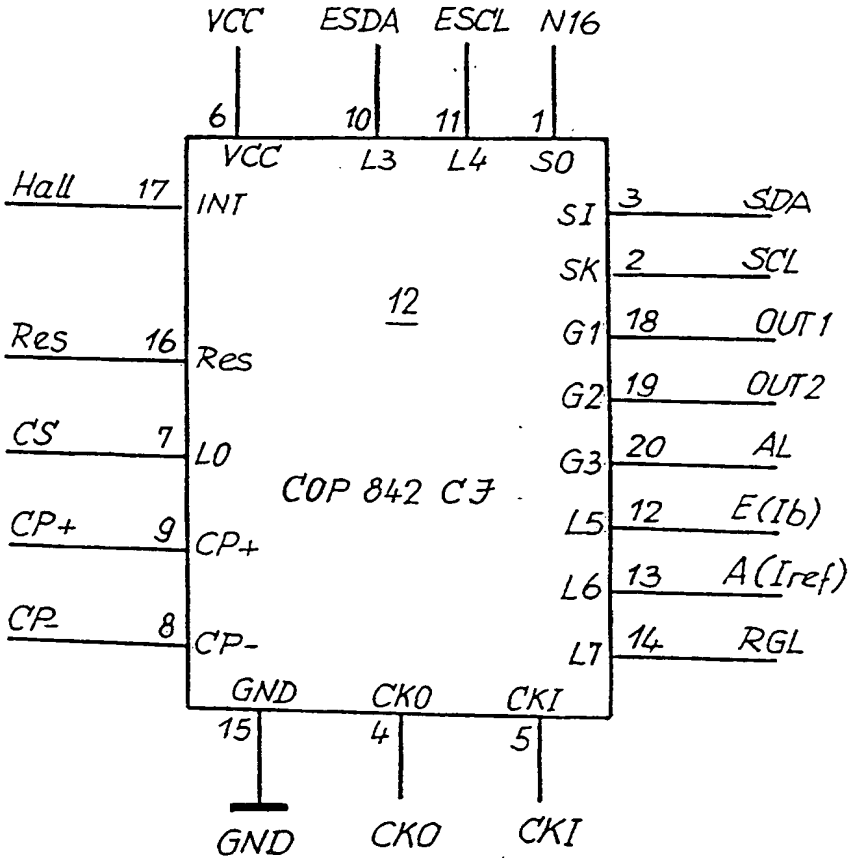

VCC
ESDA
ESCL
N16
6
10
11
1
VCC
L3
L4
SO
Hall
17
INT
SI
3
SDA
SK
2
SCL
12
Res
16
Res
G1
18
OUT1
G2
19
OUT2
CS
7
LO
G3
20
AL
COP 842 CJ
CP+
9
CP+
L5
12
E(Ib)
L6
13
A(Iref)
CP-
8
CP-
L7
14
RGL
GND
CKO
CKI
15
4
5
GND
CKO
CKI

Fig. 10

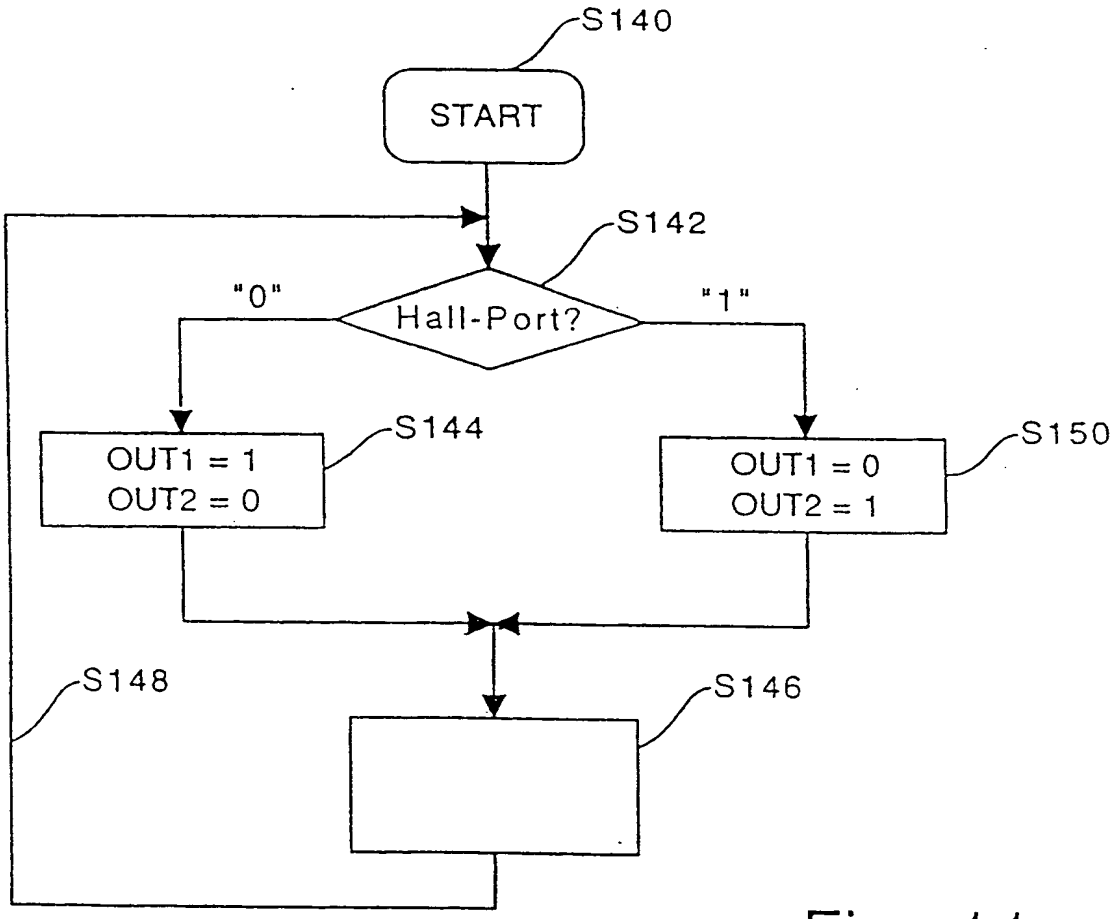
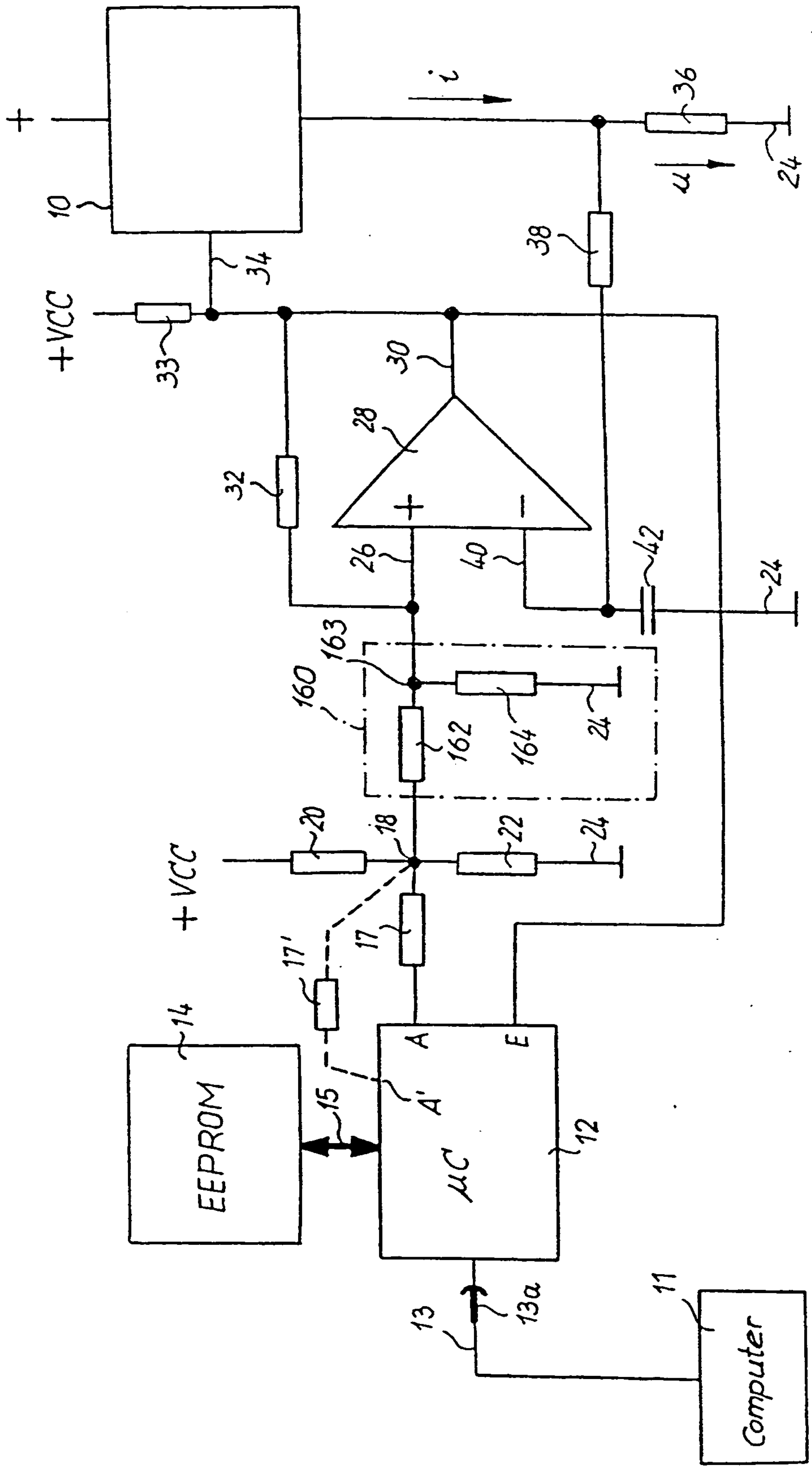

S140
START
S142
"0"
Hall-Port?
"1"
S144
OUT1 = 1
OUT2 = 0
S150
OUT1 = 0
OUT2 = 1
S148
S146

Fig. 11



+
+VCC
+VCC
i
u
EEPROM
μC
A
A'
E
Computer
10
11
12
13
13a
14
15
17
17'
18
20
22
24
26
28
30
32
33
34
36
38
40
42
160
162
163
164

Fig. 12

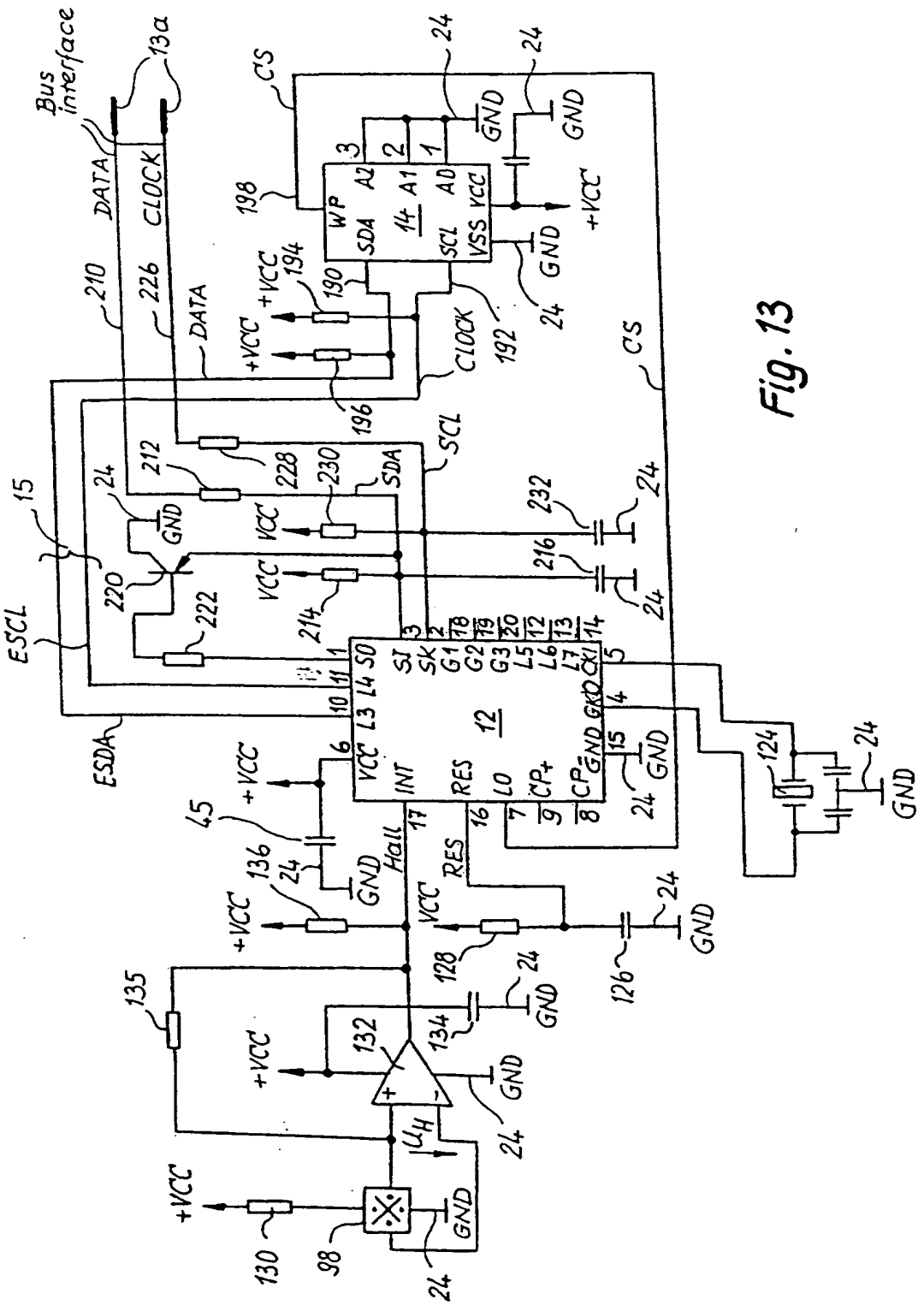

Bus interface
13a
DATA
CLOCK
CS
SCL
SDA
ESCL
ESDA
+VCC
GND
Hall
RES
CLOCK
DATA
WP
SDA
SCL
VSS
VCC
A0
A1
A2
SI
SK
SO
INT
LO
CP+
CP-
GKI
GKO
12
14
15
45
98
124
126
128
130
132
134
135
136
190
192
194
196
198
210
212
214
216
220
222
226
228
230
232

Fig. 13

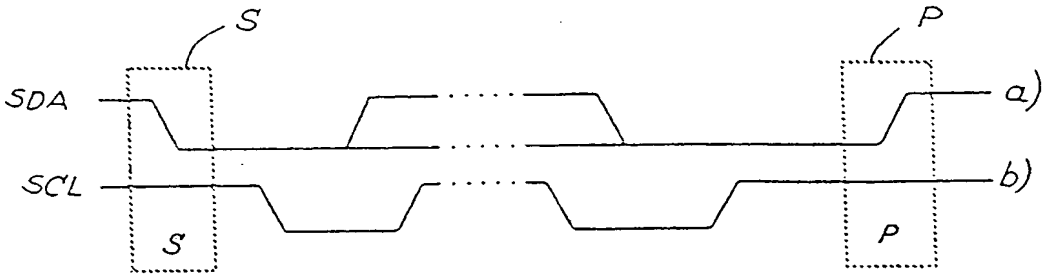


Fig. 14

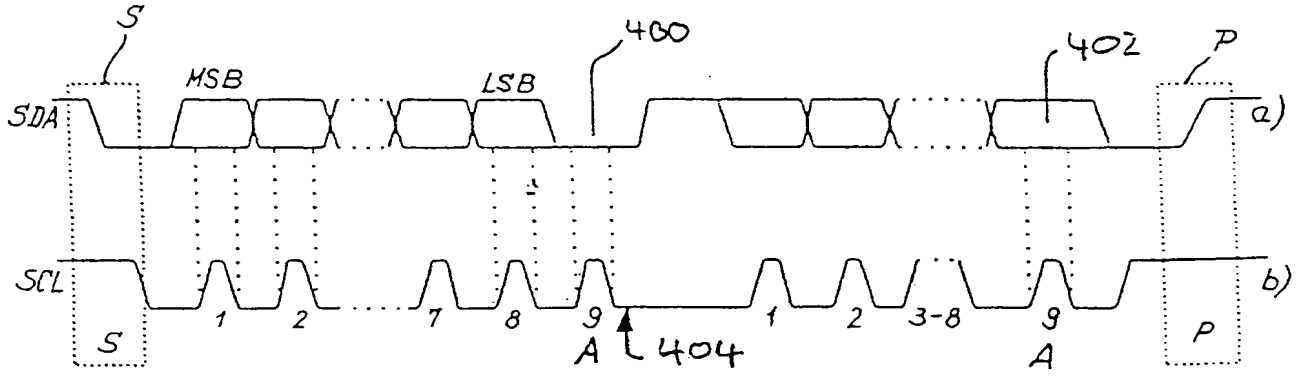


Fig. 15

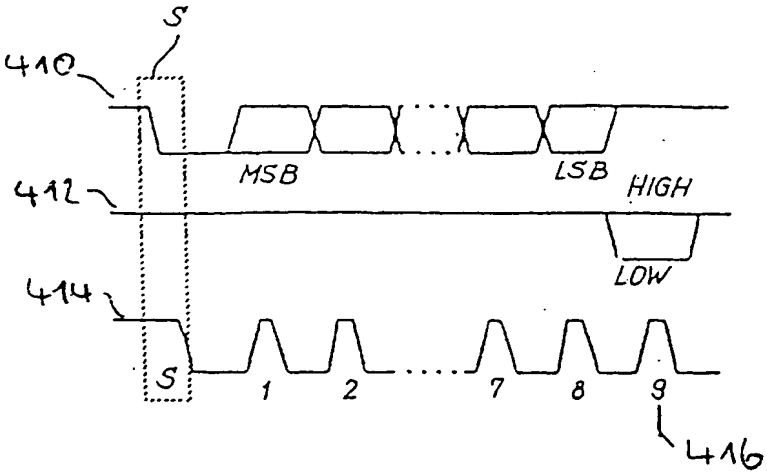


Fig. 16

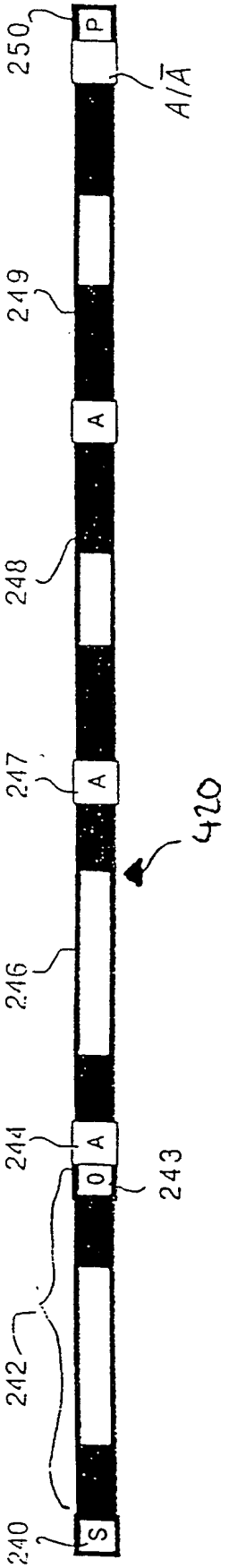

250
P
A/Ā
219
A
248
217
A
420
216
244
A
0
243
242
240
S

Fig. 17

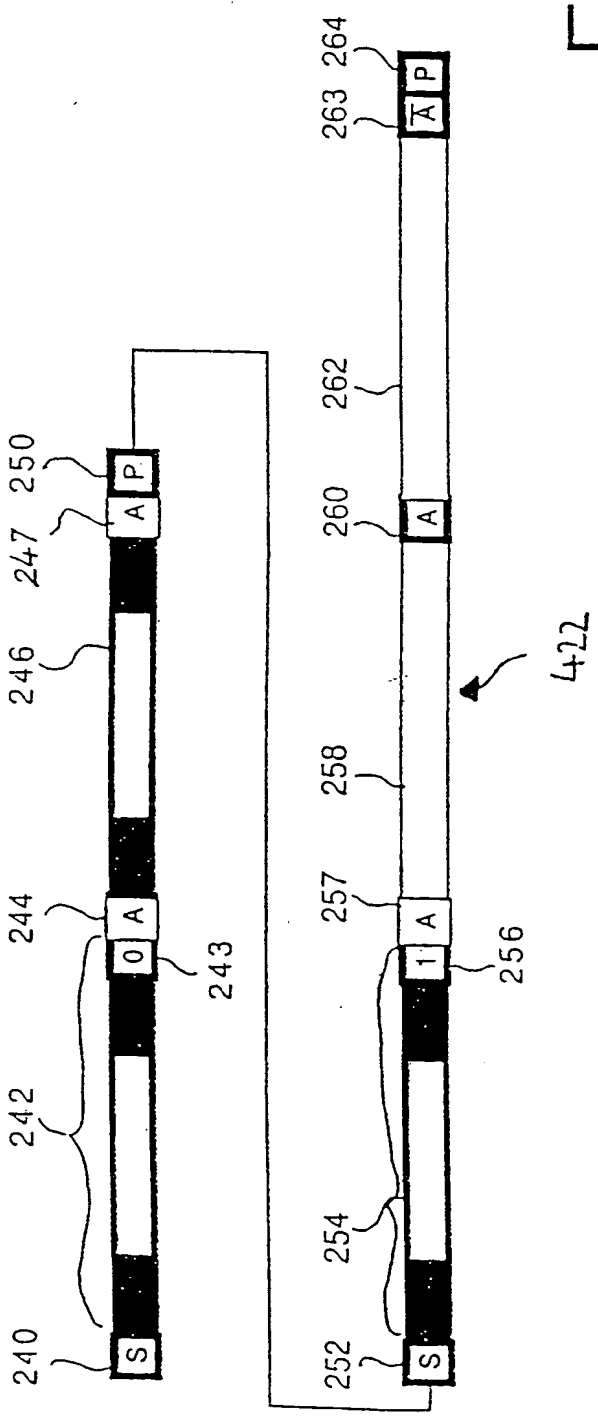

263 264
Ā P
262
260
A
422
258
257
A
1
256
254
252
S
247 250
A P
246
244
A
0
243
242
240
S

Fig. 18

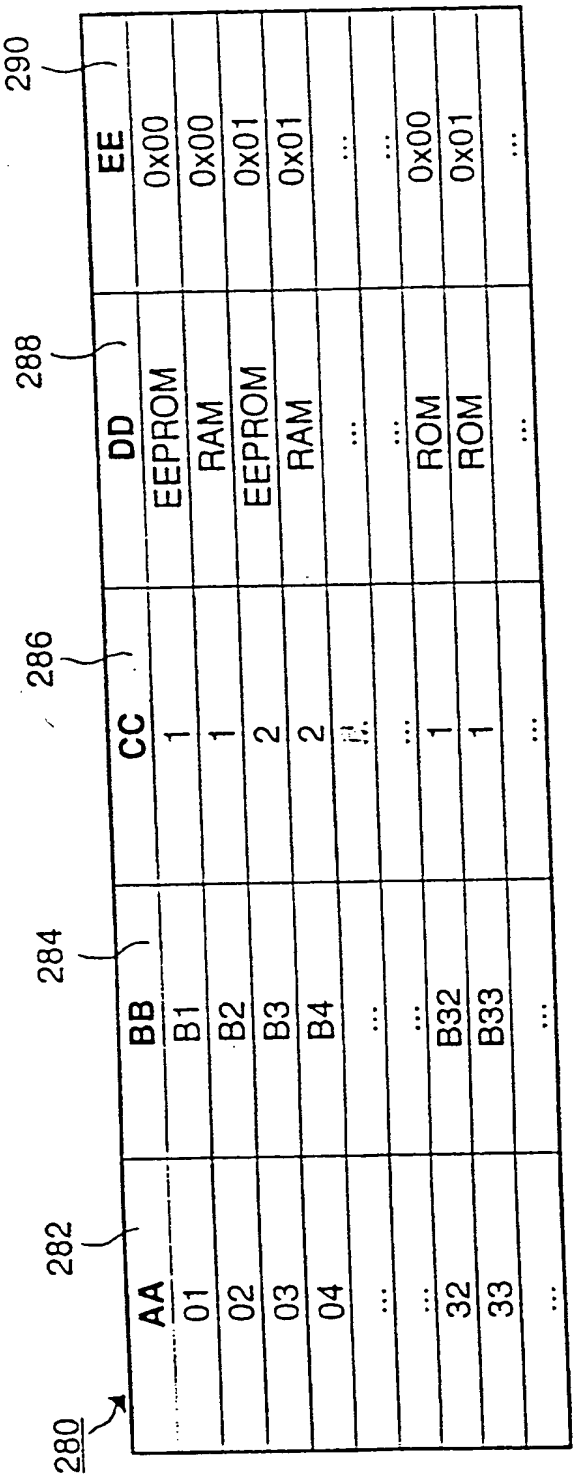


Fig. 19

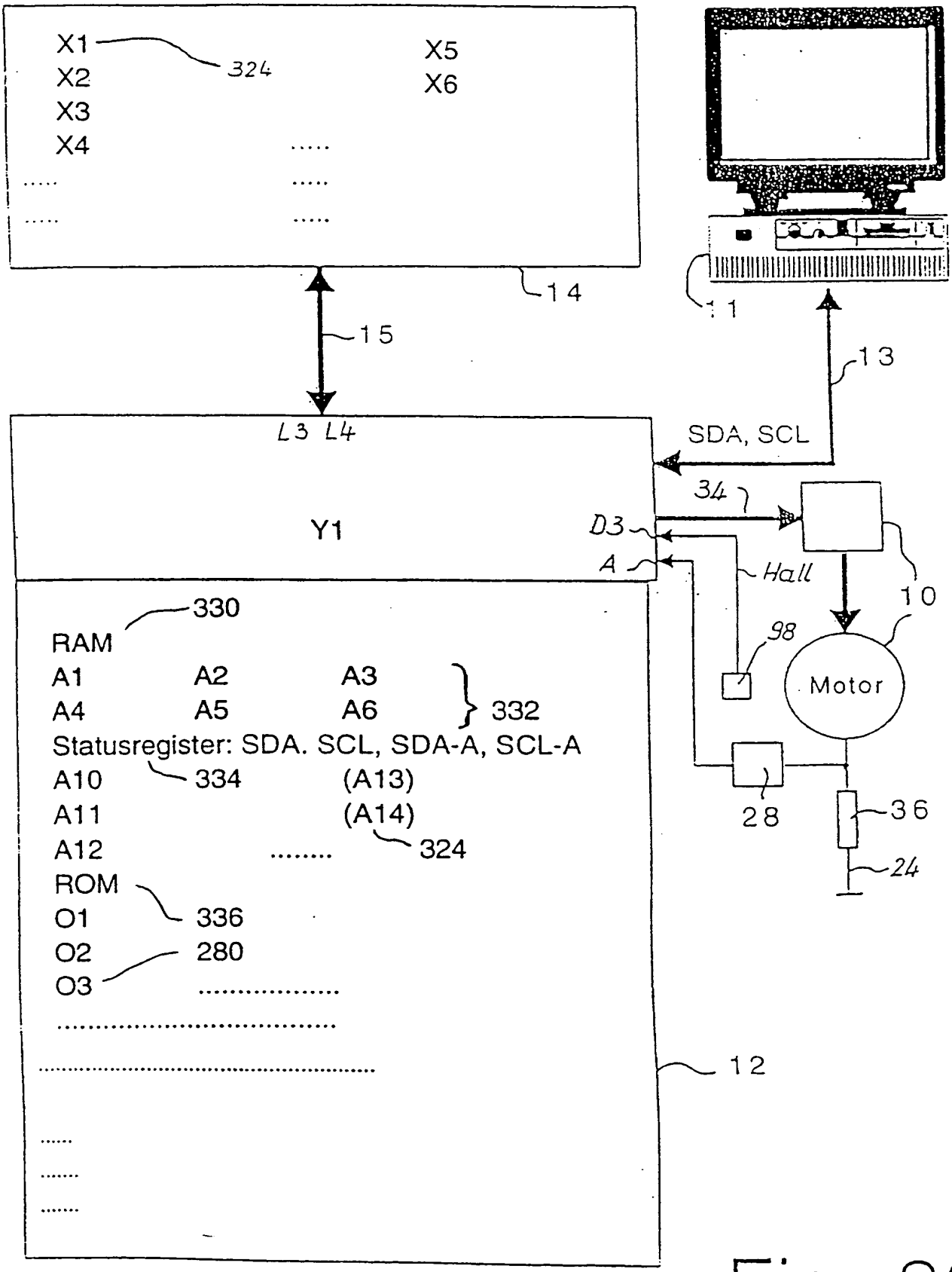

X1
X2
X3
X4
324
X5
X6
14
11
15
13
L3 L4
SDA, SCL
34
Y1
D3
A
Hall
10
98
Motor
28
36
24
330
RAM
A1 A2 A3
A4 A5 A6
332
Statusregister: SDA. SCL, SDA-A, SCL-A
A10 334 (A13)
A11 (A14)
A12 324
ROM
O1 336
O2 280
O3
12

Fig. 20

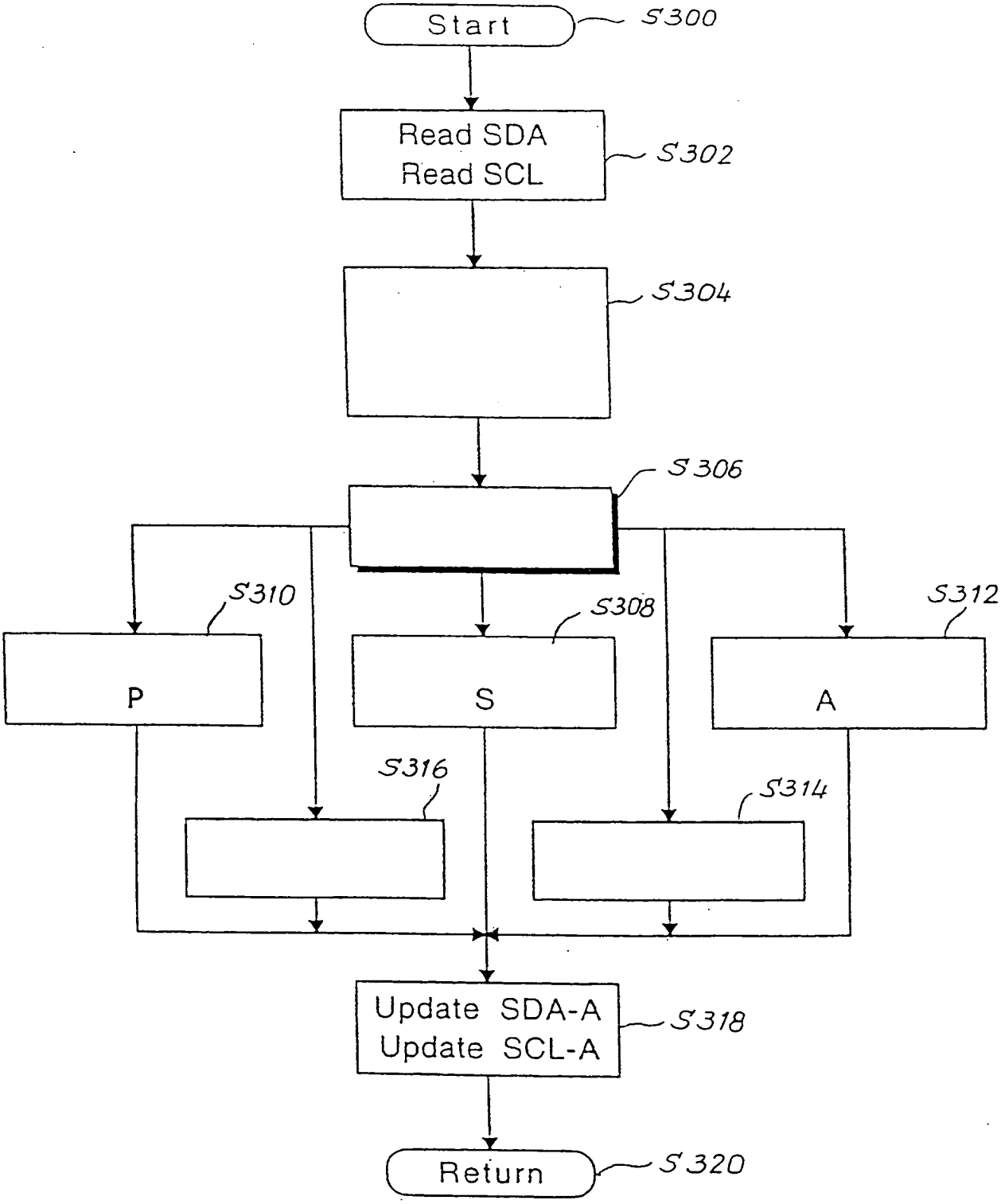

Start
S300
Read SDA
Read SCL
S302
S304
S306
S310
S308
S312
P
S
A
S316
S314
Update SDA-A
Update SCL-A
S318
Return
S320

Fig. 21

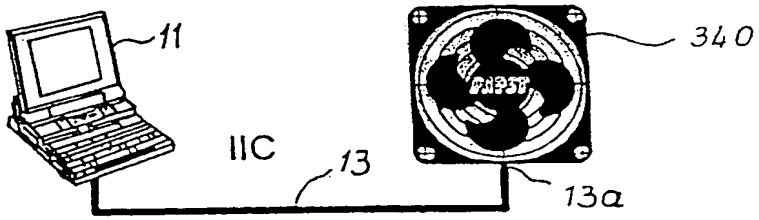

11
340
IIC
13
13a

Fig. 22

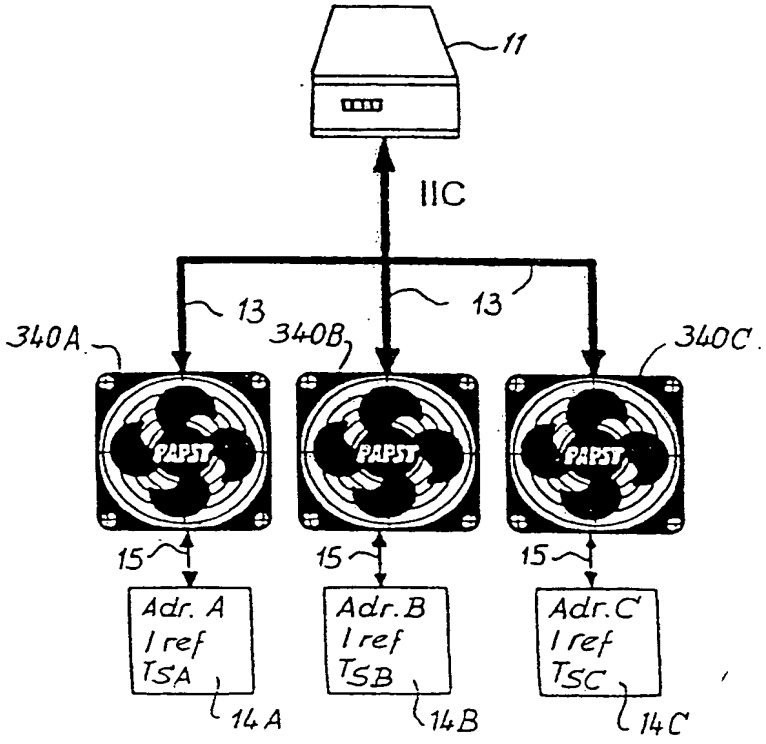

11
IIC
13
13
340A
340B
340C
15
15
15
Adr. A
I ref
TSA
Adr.B
I ref
TSB
Adr.C
I ref
TSC
14A
14B
14C

Fig. 23

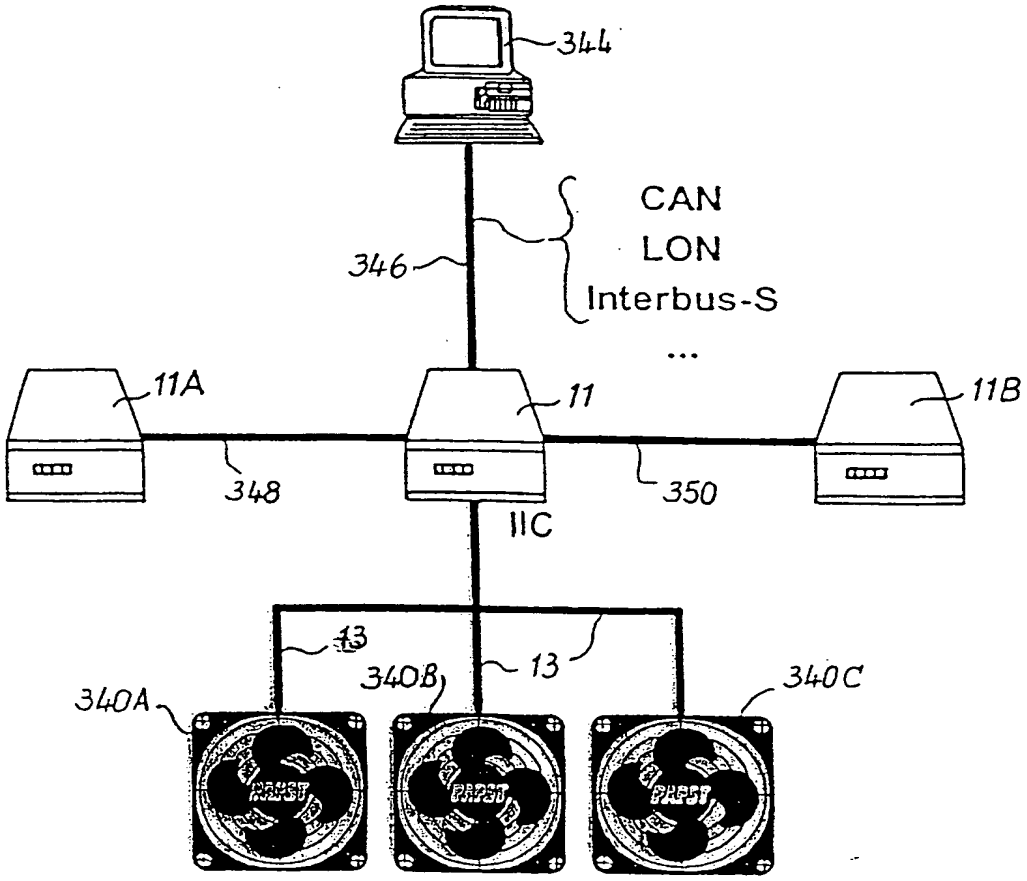

344
CAN
LON
Interbus-S
...
346
11A
11
11B
348
350
IIC
13
13
340B
340A
340C

Fig. 24